Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-7 (canceled)

Claim 8. (new) An arrangement including an analog amplifier having an input port for receiving a first signal and a test input port for receiving test signal, the analog amplifier further comprising a control input port and an output port,

the analog amplifier responsive to a first and a second condition present at the control input port, such that when the first condition is present at the control input port, the output port is operably connected to the input port and when the second condition is present at the control input port the output port is operably connected to the test input port.

Claim 9. (new) The arrangement of claim 8, wherein the first condition present at the control input port is a first control signal and the second condition present at the control input port is a second control signal.

Claim 10. (new) The arrangement of claim 8, further comprising:

a load device operably connected to the output port and selectively connectable to a first voltage;

a transistor having a first, a second and a third terminal, the first terminal selectively connectable to the input port, the second terminal operably connected to the output port and the load device; and

a tail current sink transistor operably connected to the third terminal and having a terminal selectively connectable to a biasing voltage, such that when the first condition is present at the control input port, biasing voltage is supplied to the terminal of the tail current transistor, the load device is connected to the first voltage and the first terminal is connected to the input port, and when the second condition is present at the control input port, biasing voltage is not supplied to the terminal of the tail current transistor, the load device is not connected to the input port and the first terminal is disconnected from the input port.

Claim 11. (new) The arrangement of claim 10, further comprising;

a negative biasing voltage selectively connectable to the terminal of the tail current sink transistor, such that when the second condition is present at the control input port, the terminal of the tail current sink transistor is operably connected to the negative biasing voltage.

Claim 12. (new) The arrangement of claim 10, wherein the load device is selectively connectable to the test input port, such that when the second condition is present at the control input port, the load device is operably connected to the test input port.

Claim 13. (new) The arrangement of claim 8, wherein the amplifier is a fully differential amplifier.

Claim 14. (new) The arrangement of claim 8, further comprising;

a test pattern generator operatively connected to the test input port.

Claim 15. (new) The arrangement of claim 8, wherein the test input port is capable of operable connection to an external test pattern generator.

Claim 16. (new) A method of switching the connectivity of an output port of an analog amplifier from an input port to a test input port, comprising the steps of:

providing an amplifying transistor operably connected to the output port;

providing power to the amplifying transistor;

providing a tail current sink transistor having a terminal, the tail current sink transistor operably connected to the amplifying transistor and having a biasing voltage applied to the terminal;

providing a control signal;

connecting the test input port to the output port;

disconnecting the amplifying transistor from the power; and

reducing the biasing voltage at the terminal of the tail current sink transistor;

Claim 17. (new) The method of claim 16, wherein the step of reducing the biasing voltage comprises the step of

removing the biasing voltage from the terminal of the tail current sink transistor.

Claim 18. (new) The method of claim 16, further comprising, after the step of providing a control signal, the step of

applying a negative biasing voltage to the terminal of the tail current sink transistor.

Claim 19 (new) The method of claim 16, wherein the step of providing power to the amplifying transistor comprises the step of:

providing power to the amplifying transistor through a load device, and wherein the step of connecting the test input port to the output port comprises the step of:

connecting the test input port to the output port through the load device.